(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 872 793 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
21.10.1998 Bulletin 1998/43

(51) Int. Cl.[6]: G06F 3/147, G09G 3/20, G06F 1/24

(21) Application number: 98200118.2

(22) Date of filing: 11.06.1991

(84) Designated Contracting States:
DE GB

(30) Priority: 18.06.1990 JP 159416/90

(62) Document number(s) of the earlier application(s) in accordance with Art. 76 EPC:
91910637.7 / 0 487 742

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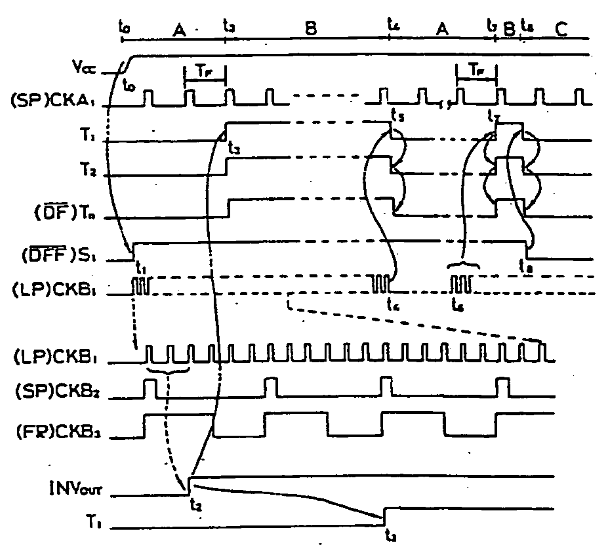
Remarks:
This application was filed on 19 - 01 - 1998 as a divisional application to the application mentioned under INID code 62.

(54) Flat display device and display body driving device

(57) In a flat panel, e.g. in an liquid crystal display, there is a need to avoid the rush current occurring when voltage supply is started on power up or resumed after a forced stop that was carried out for some reasons (e.g. for preventing damages caused by faulty connection between physically distinct and separately disposed display controller and display unit).

In order to solve such problems, in the present invention, the drivers in the display unit, receive a power on logic signal, on detection of which voltage supply is started/resumed by supplying a power control signal to the power source after a certain delay, such to avoid transient rush current.

FIG. 4



A : liquid crystal drive inhibit period
B : liquid crystal drive period
C : display-off period

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source. In response to stopping of the oscillating signal, the stoppage detection circuit sets the output signals from the control circuit corresponding to all of the electrodes to a common value.

Both of these known systems suffer from the disadvantage that only the basic oscillating signal used to drive the entire system is monitored. In practice, even if this basic oscillating signal is being produced, it is still possible for DC driving of the display to occur.

Expanding the problem about the DC drive of the liquid crystal display body, this can be generalised to a problem associated with a signal abnormality on the side of the liquid crystal module unit. Besides, in case of a wall-mounted TV, because of a display control unit and a display panel being disposed in remote places, a problem in terms of deteriorating the display quality is produced due to attenuation of signal level and influences of noises as well as to a stop of signal. Further, the problems also happen not only in the liquid crystal displays but also plasma displays.

According to a first aspect of the present invention there is provided a method of controlling a flat display unit comprising a flat display panel driven in accordance with display driving voltages, display driver means for selecting the display driving voltages supplied to the flat display panel and a display power source circuit for supplying the display driving voltages to the display driver means in response to a power control signal, the method of controlling the flat display unit comprising the steps of:

detecting a logic power voltage activating a logic circuit of the flat display unit by the display driver means;
supplying the power control signal, from the display driver means to the power source circuit, said power control signal having a delay time after the detection of said logic power voltage;
supplying the display driving voltages to the display driver means in response to the power control signal by the power source circuit; and
selecting the display driving voltages supplied from the power source circuit to the flat display panel by the display driver means.

According to a second aspect of the present invention there is provided a method of controlling a flat display device comprising a flat display panel module unit and a display control unit for supplying control signals to control display of the flat display panel module unit, said flat display panel module unit including a flat display panel driven in accordance with display driving voltages, display driver means for selecting the display driving voltages to the flat display panel and a display power source circuit for supplying the display driving voltages to the display driver means in response to a power control signal, the method of controlling the flat display unit comprising the steps of:

supplying the power control signal to the power source circuit by the display driver means, the power control signal having a delay time after a logic power voltage has supplied to a logic circuit of the flat display device;
supplying the display driving voltages to the display driver means in response to the power control signal by the power source circuit;
supplying a display start signal controlling a start of the selection of the display driving voltages by the display driver means in response to the control signal supplied from the display control unit, said display start signal having a delay time after the power control signal has supplied to the power source circuit; and
selecting the display driving voltages supplied from the power source circuit to supply to the flat display panel in response to the display start signal.

According to a third aspect of the present invention there is provided a flat display unit comprising:

a flat display panel for being driven in accordance with display driving voltages;
display driver means for selecting the display driving voltages supplied to said flat display panel, said display driver means comprising a logic circuit and a detection means for detecting a logic power voltage activating said logic circuit and for supplying a power control signal having a delay time after the detection of the logic power voltage; and
a display power source circuit for supplying the display driving voltages to said display driver means in response to the power control signal.

According to a fourth aspect of the present invention there is provided a flat display device comprising a flat display panel module unit and a display control unit for supplying control signals to control display of the flat display panel module unit,

said flat display panel module unit comprising:

a flat display panel driven in accordance with display driving voltages;
display driver means for selecting the display driving voltages supplied to said flat display panel and for supplying a power control signal having a delay time after a logic power voltage has been supplied to a logic circuit of said display driver means; and
a display power source circuit for supplying the display driving voltages to said display driving means in response to the power control signal,

wherein said display driver means starts the selection of the display driving voltages in response to a display start signal having a delay time after the power control signal has supplied to said power source circuit.

going display body driving means with the signal management control function can be constructed as a semiconductor integrated circuit. Y drivers LSI among the drivers LSI are smaller in the number of I/O wires than X drivers LSI. Taking this fact into consideration, it is advantageous that the Y drivers are employed as the drivers LSI with the signal management control function. The liquid crystal display devices are classified roughly into a simple matrix type and an active matrix type. The drivers LSI with the signal management control function are desirably scan drivers or gate drivers.

Brief Description of the Drawings:

FIG. 1 is a block diagram illustrating a whole configuration of a liquid crystal display device in an embodiment 1 of this embodiment;
FIG. 2 is a circuit diagram showing constructions of respective scan drivers and connective relations between drivers in the same embodiment;
FIG. 3 is a circuit diagram illustrating scan electrode driving cells of the scan driver in the same embodiment;
FIG 4 is a timing chart, showing relations between a variety of signals in a liquid crystal display body module unit, of assistance in explaining the operation of the same embodiment;
FIG. 5 is a block diagram depicting a whole configuration of the liquid crystal display device in a embodiment 2 of this invention;
FIG. 6 is a circuit diagram showing constructions of the signal management control units of the respective scan drivers and connective relations between the drivers in the same embodiment;
FIG. 7 is a circuit diagram illustrating a construction of a liquid crystal power source circuit in the same embodiment;
FIG. 8 is a timing chart, showing relations of a variety of signals in the liquid crystal display body module unit, of assistance in explaining the operation of the same embodiment; and
FIG. 9 is a block diagram depicting a configuration of a conventional liquid crystal display device.

Best Mode for Carrying out the Invention:

Embodiments of the present invention will hereinafter be described with reference to the accompanying drawings.

(Embodiment 1)

FIG. 1 is a block diagram illustrating a whole configuration of a liquid crystal display device in an embodiment 1 of this invention. Note that in FIG. 1, the same components as those of FIG. 9 are marked with the like reference symbols, and the description thereof will be omitted.

Signal management control units 47 are incorporated into scan driver semiconductor integrated circuits (LSI) 46_1 - 46n combined to constitute a scan electrode driving circuit (Y drivers) of a liquid crystal display module unit 40 in this embodiment. A signal management control unit 47_1 of the first scan driver semiconductor integrated circuit 46_1 detects a stop of a scanning line synchronous signal YSCL (data signal latch clock LP) applied to a terminal CKB1. The signal management control unit 47_2 of the second scan driver semiconductor integrated circuit 46_2 detects a stop of a scan start pulse (frame start signal) SP applied to a terminal CKB2. A signal management control unit 47n of the n-th (e.g., third) scan driver semiconductor integrated circuit 46n detects a stop of an AC-transforming clock FR applied to a terminal CKBn. The respective signal management control units 47_1 - 47n have signal stop detection control terminals S_1 - Sn and signal stop detection terminals T_1 - Tn. A forced blank display signal $\overline{DFF}$ of a high level voltage is normally supplied from the control circuit 10 to the signal stop detection control terminal S_1 of the signal management control unit 47_1 of the first scan driver semiconductor integrated circuit 46_1. The signal stop detection terminal T_1 is connected to the signal stop detection control terminal S_2 of the signal management control unit 47_2 of the second scan driver semiconductor integrated circuit 46_2. The signal stop detection terminal T_2 of the signal management control unit 47_2 of the second scan driver semiconductor integrated circuit 46_2 is connected to a signal stop detection terminal (e.g., the signal stop detection control terminal Sn of the n-th signal management control unit 47n) of the next stage. The signal stop detection terminal Tn of the n-th signal management control unit 47n is connected to forced blank control terminals $\overline{DF}$ of the scan drivers 46_1 - 46n and the signal drivers 24_1 - 24n.

The signal management control units 47_1 - 47n of the respective scan drivers are, as illustrated in FIG. 2, cascade-connected. Configurations of the signal management control units 47_1 - 47n are the same. A detected signal of the signal management control unit 47_1 is a data signal latch clock LP applied to the terminal CKB_1. A detected signal of the signal management control unit 47_2 is a scan start pulse (frame start signal) SP applied to the terminal CKB_2. A detected signal of the signal management control unit 47n is an AC-transforming clock FR applied to the terminal CKBn.

Now, an emphasis is placed on the signal management control unit 47_1, and the construction thereof will be explained. The signal management control unit 47_1 includes a signal stop detection circuit 48 serving as a signal detection means for detecting a stop of the detected signal and a sequence processing circuit 51 consisting of a signal delay circuit 49 and a logic circuit 50.

The signal stop detection circuit 48 is composed of: a first N-type MOS transistor Tr_1 switched by a latch clock LP conceived as a detected signal and constitut-

circuit 48 assumes an on-status, whereas the transistor Tr2 assumes an off-status. Hence, the capacitor C_{11} is charged with electricity for this period. During an L-level period of the data signal latch clock LP, the transistor Tr_2 of the signal stop detection circuit 48 is in the on-status, whereas the transistor Tr_1 is in the off-status. Therefore, a part of electric charge supplied to the capacitor C_{11} is transfer-fed to a capacitor C_{12}. A charging voltage of the capacitor C_{12} increases with a generation of repetitive pulses of the data signal latch clocks LP. An input voltage of the inverter INV_2 comes to the threshold value V_{TH} or under. An output INV_{OUT} of the inverter INV_2 assumes the H level at a timing t_2. Before the timing t_2, the output INV_{OUT} of the inverter INV_2 assumes the L level. Therefore, the output Q of the D-type flip-flop 49a of the signal delay circuit 49 is at the L level. For this reason, an output T_1 of the logic circuit 50 assumes the L level. Even when the output INV_{OUT} becomes the H level at that moment, the output Q does not assume the H level at the timing t_2. During a 1-frame period (T_F) and a 2-frame period ($2T_F$) of the frame start signal SP, the output Q is kept at the L level due to delayed storage action of the input signals of the D-type flip-flops 49b, 49a. At a timing t_3, the output T_1 of the logic circuit 50 assumes the H level.

The frame start signal SP is supplied to the detection terminal CKB_2 of the signal stop detection circuit 48_2 of the signal management control unit 47_2. Supplied to an input terminal CKA_2 of the signal delay circuit 49_2 is the frame start signal SP defined as a cascade input DI_2 coming from a cascade output terminal DO of the scan driver 46_1. The output T_1 of the logic circuit 50 of the scan driver 46_1 is cascade-connected to the logic circuit 50 of the scan driver 46_2. A capacitor C_{21} of the signal stop detection circuit 48_2 is fed with an electric energy by repetitive pulses of the frame start signals SP. Similarly, the AC-transforming signal FR is supplied to a detection terminal CKBn of the signal stop detection circuit 48n of the signal management control unit 47n in the scan driver 46n. Supplied to an input terminal CKAn of the signal delay circuit 49n is the frame start signal SP defined as a cascade input DIn coming from the output terminal DO of the scan driver 46_2. The output T_2 of the logic circuit 50 of the scan driver 46_2 is cascade-connected to the logic circuit 50 of the scan driver 46n. A capacitor Cn2 of the signal stop detection circuit 48n is charged with the electricity by the repetitive pulses of the AC-transforming signals FR. Periods and duty ratios of the data signal latch clock LP conceived as a detected signal, the frame start signal SP and the AC-transforming signal FR are different. For making coincident the comparative judgment timings t3 of the inverters INV_1 - INVn in the respective scan drivers, it is desirable that values (time constants) of discharge resistances R_1 - Rn and of the capacitors C_{11} - Cn1, C_{12} - Cn2 be mutually adjustable. For this purpose, in this embodiment, as illustrated in FIG. 1, the scan driver is provided with connection external terminals of the resistances and the externally attached capacitors.

As described above, during a period from the on-timing t_0 of the logic power source Vcc to the timing t_3 when the outputs T_1 - Tn of the logic circuit assume the H level, the L level outputs Tn are supplied to the forced display blank control terminals $\overline{DF}$ of the signal drivers and the scan drivers. A liquid crystal display panel 22 is therefore in a blank display state. More specifically, when the forced display blank control signal $\overline{DF}$ is at the L level, only a transistor F_1 of the selection switch 46h of the scan electrode driving cell 46 remains in an on-state under control of the forced blank display control circuits 46b, 46d depicted in FIG. 3. A voltage of V_5 (0v) is impressed on the scan electrodes, while an inter liquid crystal electrode voltage (liquid crystal applying voltage) is 0v. A period from the timing t_0 to the timing t_3 corresponds to a liquid crystal drive inhibit period. At the timing t_1, the liquid crystal power source circuit 28 is powered on, whereby the liquid crystal voltages V_0 - V_5 are generated. Those voltages are supplied to the scan and signal drivers. At a power source actuation timing, the shift registers in the scan and signal drivers are in an unsteady state. The liquid crystal display continues to be blank-controlled up to the timing t_3, however, it is therefore possible to avoid abnormal driving of the liquid crystal panel.

Next, when the output Tn becomes the H level at the timing t_3, H-level voltages are supplied to the forced display blank control terminals $\overline{DF}$ of the scan and signal drivers. The liquid crystal display panel 22 is thereby AC-driven by normal operations of the scan and signal drivers. A display picture is depicted on the liquid crystal panel 22. The symbol B of FIG. 4 indicates a liquid crystal driving period. The liquid crystal power source circuit 28 and the logic units of the scan and signal drivers are powered on at the timing t_1. At the timing t_3 later than that timing, the liquid crystal display panel 22 is driven. Therefore, since the power-on of the power source does not take place simultaneously, an excessive power source rush current is restrained. It is because, in addition to delayed action of the signal stop detection circuit 48 itself, the delayed action of the signal delay circuit 49 having a delay time of 1 - 2 frame period functions effectively.

Now, it is presumed that an output of the data signal latch clock LP transmitted from the liquid crystal module controller 12 is stopped at a timing t_4 in the liquid crystal driving period B. During outputting of the data signal latch clock LP, the sufficient electric energy is supplied to the second capacitor C_{12} of the signal detection circuit 48_1 of the scan driver 46_1. When the clock thereof is stopped, no electric charge is transferred to the second capacitor C_{12} from the first capacitor C_{11}. Besides, the electric charge of the second capacitor C_{12} is quickly discharged at a predetermined time constant via the discharge resistance R_1. An input voltage of the inverter INV_2 is gradually boosted. If that input voltage exceeds the threshold value V_{TH}, the output voltage

next be explained with reference to FIG. 8. A power switch SW is closed at a timing t_0. The logic power source Vcc of the liquid crystal display device is turned on. As in the same way with the embodiment 1, a reset signal having a pulse width of several µs - several ms is supplied from an MPU to a power-on reset terminal RS of the liquid crystal module controller 12. The liquid crystal module controller 12 is thereby initialized. Hence, an output signal from the liquid crystal module controller 12 is generally in a stopping status. During such a period, the logic power source voltage Vcc is supplied to one input of the logic circuit 78c defined as an AND circuit of the first scan driver 76_1. The data signal latch clock LP does not yet, however, come out, and hence its output PF_1 assumes the L level. As a result, an output PF_2 of the second scan driver 76_2 is also at the L level. Besides, an output PFn of the n-th scan driver 76n becomes also the L level, whereby a power-off terminal $\overline{POFF}$ of the liquid crystal power source circuit 28 is kept at the L level. For this reason, a base potential of the transistor 28b shown in FIG. 7 assumes an L level (0v), so that a boosted voltage is not supplied to the smoothing capacitor 28d. Therefore, the liquid crystal driving voltages V_0 - V_5 are not generated. As is similar to the embodiment 1, no DC component is applied between the liquid crystal electrodes during this initializing period. A deterioration of the liquid crystal elements is prevented.

Next, as illustrated in FIG. 8, a variety of signals are generated from the liquid crystal module controller 12 at a timing t_1. The forced blank display signal $\overline{DFF}$ is changed from the L level to the H level. Generated are the frame start signal SP, the data signal latch clock LP and the AC-transforming clock FR. As explained in the embodiment 1, upon a start of appearance of the data signal latch clock LP, the output INV_{OUT} of the inverter INV_2 assumes the H level at a timing t_2. For this reason, the output Q of the power on/off control circuit 78b becomes the H level at a timing t_3 which is later by a 1 - 2 frame period than the timing t_2. The output PF_1 of the logic circuit 78c therefore becomes the H level. The outputs PF_2, PFn of the logic circuits 78c of the second and n-th scan drivers 76_2, 76n become the H level, correspondingly. The power-off terminal $\overline{POFF}$ of the liquid crystal power source circuit 28 is energized at the H level. In consequence of this, the transistor 28b is put into an on-state. The transistor 28c is also brought into the on-state because of a drop in voltage of an inter base/emitter resistance of the transistor 28c. The smoothing capacitor 28d is charged with the electricity, thereby generating the liquid crystal driving voltages V_0 - V_5. During a period from the timing t_3 to a timing t_4 when the next frame start signal SP comes, the output Q of the D-type flip-flop 79c remains at the L level. The stage number of the D-type flip-flops of the signal delay circuit 79_1 in this embodiment is greater by 1 than in the power on/off control circuit 78_1. The output Q of the D-type flip-flop 79c becomes the H level slower by a 1-frame period T_F than that of the D-type flip-flop 78b. As a result, the outputs T_1, T_2, Tn all become the H level. As in the same way with the embodiment 1, the forced blank display signal $\overline{DF}$ on the part of the liquid crystal module unit is changed from the L level to the H level. The driving voltages V_0 - V_5 are thereby supplied to the scan and signal electrodes of the liquid crystal display panel 22. The operation then enters a liquid crystal mode.

For instance, concurrently with a generation of the liquid crystal driving voltages V_0 - V_5, the liquid crystal display panel 22 is driven. It follows that large charge rush currents are induced in power source units of the scan and signal drivers as well as in the liquid crystal panel. In accordance with this embodiment, however, the liquid crystal drive is initiated after the 1-frame period T_F since the liquid crystal driving voltages V_0 - V_5 have been generated at the timing t_3. The power source units are energized with a time difference, whereby the rush currents can be dispersed. This makes it possible to prevent a power-down and reduce a power capacity, which is in turn helpful for protecting the liquid crystal display panel and the drivers as well. The above-described power control decreases a burden in terms of system development costs and restrains an increase in the number of signal wires between the conventional system and LCD module. Furthermore, a reduction in the power capacity is brought about, and hence inexpensive power source is available.

Next, supposing that oscillations of the data signal latch clocks LP transmitted from the liquid crystal module controller 12 are stopped at the timing t_5 in the liquid crystal driving period B, as in the embodiment 1, the input voltage of the inverter INV_2 is boosted. The output voltage INV_{OUT} becomes the L level at a timing t_6. The outputs T_1, T_2, Tn also become the L level. As a result, the forced display blank control signal $\overline{DF}$ on the side of the liquid crystal display module unit assumes the L level. The liquid crystal display panel 22 is thereby put into a blank display state. The effects as those of the embodiment 1 are exhibited. When the output voltage INV_{OUT} of the inverter INV_2 assumes the L level, the outputs PF_1, PF_2, PFn simultaneously become the L level. The power-off terminal $\overline{POFF}$ of the liquid crystal power source circuit 28 is changed to the L level. The liquid crystal driving voltages V_0 - V_5 cease to be generated.

The data signal latch clock LP starts reappearing at a timing t_7. As in the same way with the embodiment 1, the output voltage INV_{OUT} of the inverter INV_2 becomes the H level at a timing t_8. As discussed above, the outputs PF_1, PF_2, PFn also become the H level at a timing t_9 after the 1 - 2 frame period from that timing t_8. In consequence of this, the power-off terminal $\overline{POFF}$ of the liquid crystal power source circuit 28 is changed to the H level. Generated are the liquid crystal driving voltages V_0 - V_5 which are in turn applied to the drivers. As explained earlier, the outputs T_1, T_2, Tn become the H

rush currents can be reduced. The present invention is applicable not only to the liquid crystal display device but also to a plasma display device and the like. The present invention is suitable for use with display devices where the display quality and life-span of the display body are unrestorable due to the abnormality in the driving signals.

Claims

1. A method of controlling a flat display unit comprising a flat display panel driven in accordance with display driving voltages, display driver means for selecting the display driving voltages supplied to the flat display panel and a display power source circuit for supplying the display driving voltages to the display driver means in response to a power control signal, the method of controlling the flat display unit comprising the steps of:

   detecting a logic power voltage activating a logic circuit of the flat display unit by the display driver means;
   supplying the power control signal from the display driver means to the power source circuit, said power control signal having, a delay time after the detection of said logic power voltage;
   supplying the display driving voltages to the display driver means in response to the power control signal by the power source circuit; and
   selecting the display driving voltages supplied from the power source circuit to the flat display panel by the display driver means.

2. The method according to Claim 1, further comprising the step of supplying a start signal controlling a start of display to the display driver means after supplying the display driving voltages to the display driver means.

3. A method of controlling a flat display device comprising a flat display panel module unit and a display control unit for supplying control signals to control display of the flat display panel module unit, said flat display panel module unit including a flat display panel driven in accordance with display driving voltages, display driver means for selecting the display driving voltages to the flat display panel and a display power source circuit for supplying the display driving voltages to the display driver means in response to a power control signal, the method of controlling the flat display unit comprising the steps of:

   supplying the power control signal to the power source circuit by the display driver means, the power control signal having a delay time after a logic power voltage has supplied to a logic circuit of the flat display device;
   supplying the display driving voltages to the display driver means in response to the power control signal by the power source circuit;
   supplying a display start signal controlling a start of the selection of the display driving voltages by the display driver means in response to the control signal supplied from the display control unit, said display start signal having a delay time after the power control signal has supplied to the power source circuit; and
   selecting the display driving voltages supplied from the power source circuit to supply to the flat display panel in response to the display start signal.

4. The method according to Claim 3, wherein the flat display panel module unit is arranged separately from the display control unit.

5. A flat display unit comprising:

   a flat display panel for being driven in accordance with display driving voltages;
   display driver means for selecting the display driving voltages supplied to said flat display panel, said display driver means comprising a logic circuit and a detection means for detecting a logic power voltage activating said logic circuit and for supplying a power control signal having a delay time after the detection of the logic power voltage; and
   a display power source circuit for applying the display driving voltages to said display driver means in response to the power control signal.

6. A flat display device comprising a flat display panel module unit and a display control unit for supplying control signals to control display of the flat display panel module unit,

   said flat display panel module unit comprising:
   a flat display panel driven in accordance with display driving voltages;
   display driver means for selecting the display driving voltages supplied to said flat display panel and for supplying a power control signal having a delay time after a logic power voltage has been supplied to a logic circuit of said display driver means; and
   a display power source circuit for supplying the display driving voltages to said display driving means in response to the power control signal,
   wherein said display driver means starts the selection of the display driving voltages in response to a display start signal having a delay time after the power control signal has supplied to said power source circuit.

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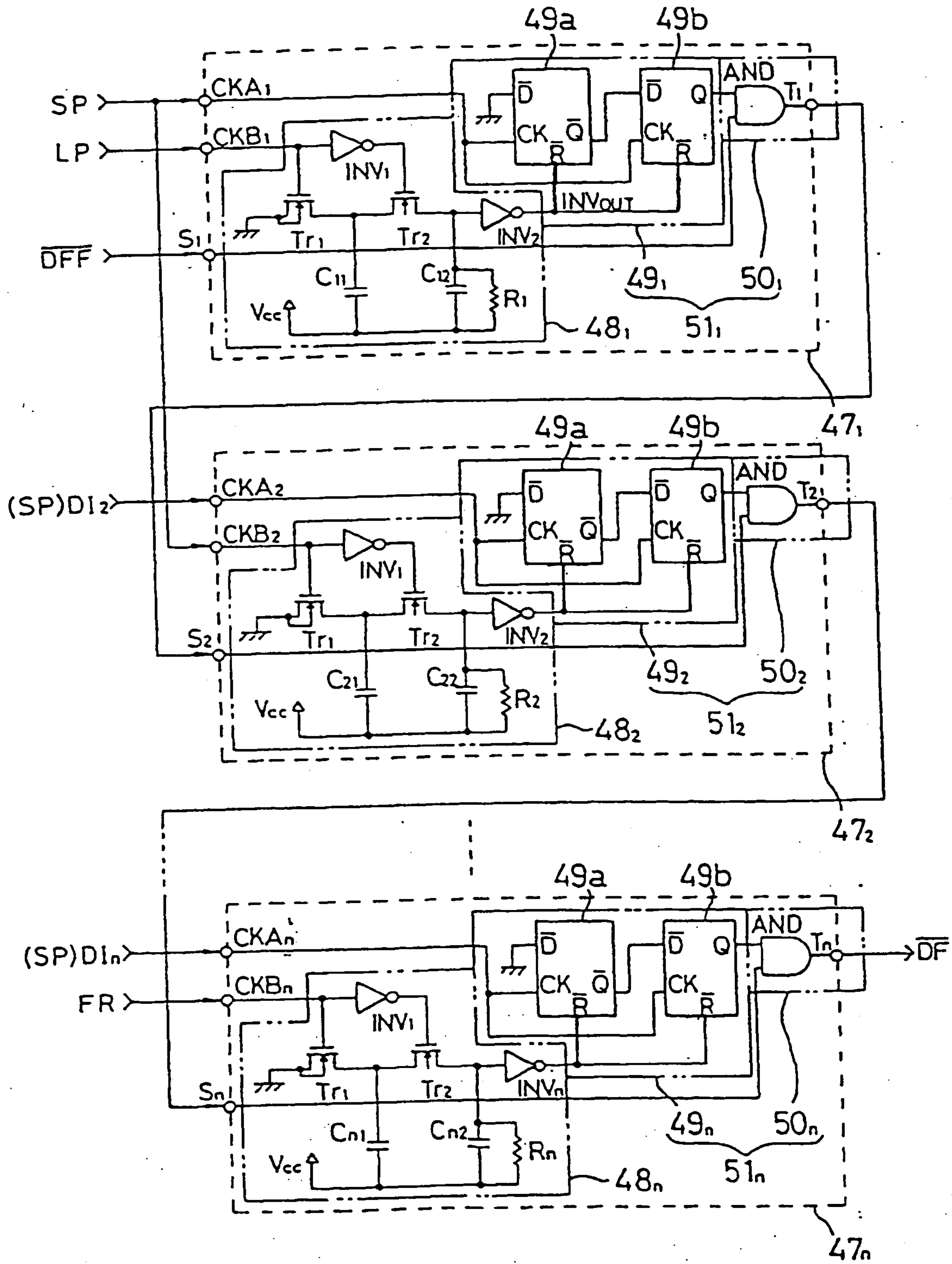
49a
49b
AND
SP
LP
DFF
CKA1
CKB1
S1
INV1
INV2
INVOUT
Tr1
Tr2
C11
C12
R1
Vcc
T1
49₁
50₁
51₁
48₁
47₁
(SP)DI2
CKA2
CKB2
S2
C21
C22
R2
T2
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50₂
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47₂
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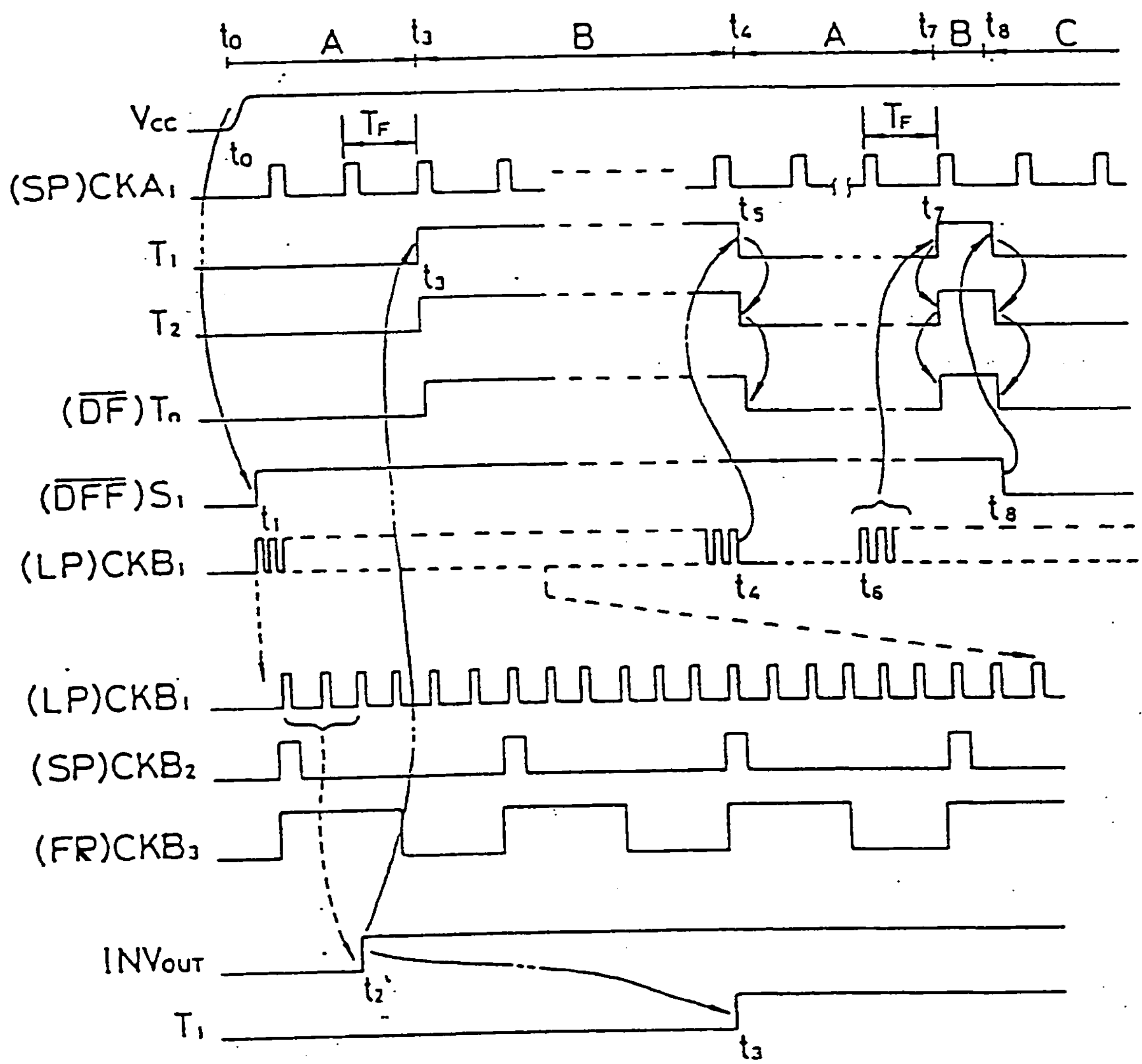
51n
48n
47n

FIG. 4



A : liquid crystal drive inhibit period

B : liquid crystal drive period

C : display-off period

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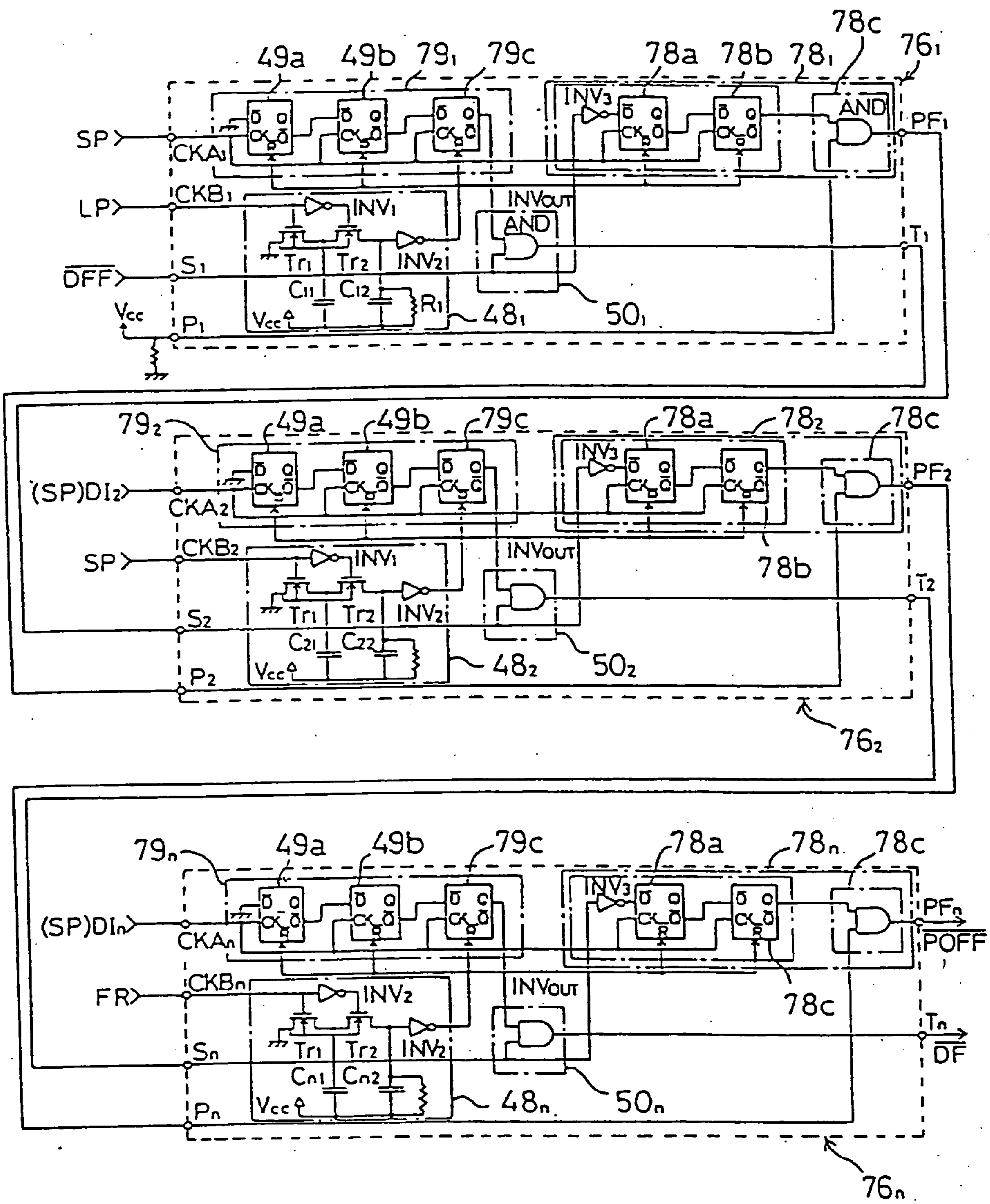

78c
49a
49b
79₁
79c
78a
78b
78₁
76₁
INV₃
AND
SP
CKA₁
PF₁
LP
CKB₁
INV₁
INVOUT
AND
Tr₁
Tr₂
INV₂
T₁
DFF
S₁
C₁₁
C₁₂
R₁
Vcc
P₁
48₁
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79₂
49a
49b
79c
78a
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78c
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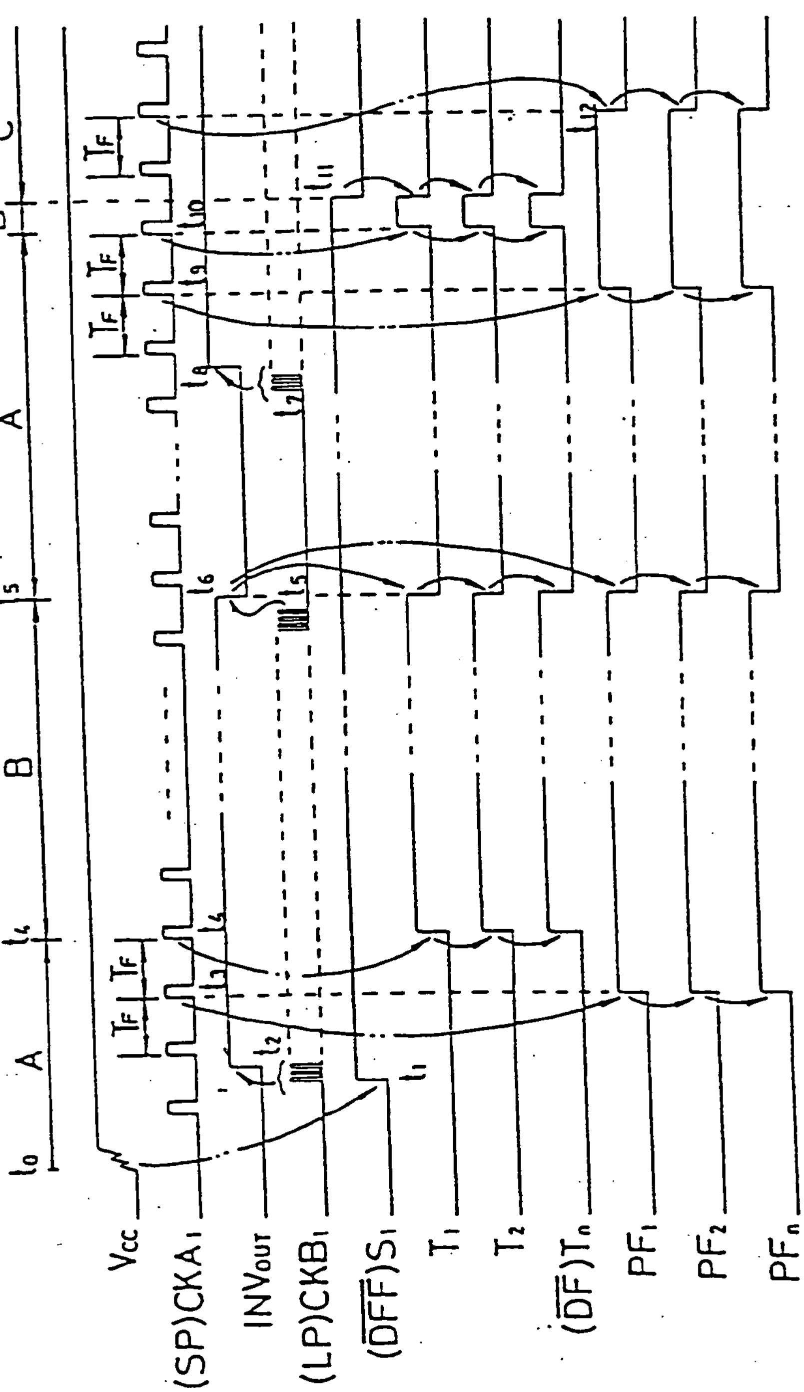
FIG. 8



A : liquid crystal drive inhibit circuit

B : liquid crystal drive period

C : display-off period

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 98 20 0118

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	WO 88 07250 A (THE CHERRY CO.) 22 September 1988 * Asbtract * * page 7, line 22 - page 10, line 33; figure 1 *	1-6	G06F3/147 G09G3/20 G06F1/24
A	US 3 894 247 A (DE JONG) 8 July 1975 * Abstract * * column 1, line 1 - line 11; figures 1,2 * * column 2, line 6 - column 3, line 14 * * column 6, line 24 - line 46 *	1-6	
A	EP 0 285 401 A (CANON K.K.) 5 October 1988 * Abstract * * page 33, line 23 - page 35, line 19; figures 33,34 *	1-6	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			G06F G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	26 August 1998	Corsi, F

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)